SANTHIRAM ENGINEERING COLLEGE, NANDYAL (AUTONOMOUS)

Approved by AICTE, New Delhi, Permanently Affiliated to JNTUA, Ananthapuramu
Accredited by NAAC (Grade-A), Accredited by NBA (ECE & CSE)
An ISO 9001: 2015 Certified Institution, 2(f) & 12(B) recognition by UGC Act, 1956
NH-40, NANDYAL-518501 (Dist), A.P.

Learn - Grow - Empower

ACADEMIC REGULATIONS, COURSE STRUCTURE AND DETAILED SYLLABI

M.TECH

Regular Two Year PG Degree Course

(Applicable for the Batches Admitted from 2023-24)

R-23

16 Years of Excellence

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SANTHIRAM ENGINEERING COLLEGE::NANDYAL

ACADEMIC RULES & REGULATIONS

(Effective for the students admitted into I year from the Academic Year 2023-2024)

1. Eligibility Criteria for M.Tech Admission:

i. Admission into the M. Tech Program shall be made subject to the eligibility, qualification and specialization prescribed by the A.P. State Government/ University from time to time.

ii. Admissions shall be made either on the basis of the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECET) for M.Tech. programmes/ an entrance test conducted by university/on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

2. Award of the M. Tech Degree

A student shall be declared eligible for award of degree, if he/she fulfils the following academic regulations:

i. Effective from the academic year 2023-24.
ii. Pursued a course of study for not less than two academic years and not more than four academic years.
iii. Registers for 70 credits and secures all 70 credits.
iv. The minimum days in each semester are 90.
v. A student who secures highest percentage of marks in the batch will be honored with gold medal.
vi. A student who secures second highest percentage of marks in the batch will be honored with silver medal.

3. Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M.Tech. course and their admission stands cancelled.

4. Programme of Study:

The following program of study are offered at present for specialization in the M. Tech as given in Table1.

Table 1: Program Offered

S.No	Discipline	Specialization	Program code
1	Electronics & Communication Engineering	VLSI System Design	57

5. Programme related terms:

i. Credit: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (Lecture/Tutorial) or two hours of practical work/field work per week.

Credit definition:

1 Hr. Lecture (L) per week	1 credit
1 Hr. Tutorial (T) per week	1 credit
1 Hr. Practical (P) per week	0.5 credit
4 Weeks of MOOCs Course	1 Credit

i. **Academic Year:** Two consecutive (one odd + one even) semesters constitute one academic year.

ii. **Choice Based Credit System (CBCS):** The CBCS provides choice for students to select from the prescribed courses.

6. Programme Pattern

i. Total duration of the M.Tech. programme is two academic years

ii. Each academic year of study is divided into two semesters.

iii. Calendar for any semester shall be announced at least two weeks before its commencement.

iv. The student shall not take more than four academic years to fulfill all the academic requirements for the award of M.Tech degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M.Tech. programme.

v. The medium of instruction of the programme (including examinations and project reports) will be in English only.

vi. All subjects/courses offered for the M.Tech degree programme are broadly classified as follows: Core Courses, Elective courses, Mandatory Courses, Research & Audit Courses. The curriculum shall be approved by corresponding Board of studies & academic council.

vii. Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

viii. Internships which can be conducted during IV semester, and same may be evaluated at end of the IV semester.

ix. The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters.

x. All subjects/courses offered for the M. Tech programme are broadly classified as given in Table 2 & 3.

Table 2: Subject Course Classification

S.No.	Broad Course Classification	Course Category	Description
1.	**Core Courses**	Program Core (PC)	Includes subjects related to the parent discipline/department/branch of Engineering
2.	**Elective Courses**	Program Specific Elective (PE)	Includes elective subjects related to the parent discipline/department/ branch of Engineering
		Open Elective (OE)	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline which are of importance in the context of special skill development
3.	**Research**	Project Work (PW)	M.Tech. Project or Major Project
		Technical Seminar	Ensures preparedness of students to undertake major projects/Dissertation, based on core contents related to specialization
		Internships	Industry Oriented Internship
		Co-curricular Activities	Attending conferences, scientific presentations and other scholarly activities
4.	**Audit Courses (MC)**	Audit Courses (Mandatory Non-credit courses)	Covering subjects of developing desired attitude among the learners is on the line of initiatives such as Unnat Bharat Abhiyan, Yoga, Value education etc.

Table 3: Category wise distribution of credits

S. No.	Name of the Program	Breakup of Credits
1	Program Core Courses (**PC**)	20
2	Program Electives Courses (**PE**)	15
3	Open Elective Courses (**OE**)	03
4	Mandatory Courses (**MoC**)	02
5	Audit Courses (**AC**)	Non-Credit
6	Project Work (**PW**), Technical Seminar, Industry Internship,Co-Curricular Activities	30
Total Credits		**70**

7. Semester Structure:

Each academic year is divided into TWO semesters (one odd + one even). Each semester shall be of 16 weeks duration and this period includes time for registration of courses, course work, examination preparation, and conduct of examinations.

Apart from the regular semester end examinations, the college will also schedule and conduct **supplementary examinations** for all courses for the student with backlogs. Such

students, who are writing supplementary examinations as supplementary candidates, may have to write more than one examination per day.

8. Attendance Requirements:

i. A student shall be eligible to appear for the University external examinations if he/she acquires i) a minimum of 50% attendance in each course and ii) 75% of attendance in aggregate of all the courses.

ii. Condonation of shortage of attendance in aggregate up to 10% (A minimum of 40% in each course and 65% and above but below 75% in aggregate) in each semester may be granted by the College Academic Committee.

iii. Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence

iv. A student with attendance less than 40% in any course and/ or less than 65% attendance in aggregate in a semester shall not be condoned in any case. Therefore, the student will be detained for that semester.

v. Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class.

vi. A stipulated fee shall be payable towards condonation of shortage of attendance.

vii. A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek re-admission into that semester when offered next.

viii. If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

ix. If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

9. Assessment and Evaluation Pattern:

The performance of a student in each course shall be evaluated based on Continuous Internal Evaluation (CIE) and Semester End Examination (SEE). The evaluation pattern is given in Table 4.

Table 4: Evaluation Pattern

S.No	Category of course	Marks		
		CIE	SEE	TOTAL
1	Theory courses	40	60	100
2	Laboratory or Practical courses	40	60	100
3	Mandatory courses	40	60	100
4	Audit(Mandatory Non-credit Courses)	40	------	40
5	Industrial Internship	100	------	100
6	Project work- Phase-I	100	------	100
7	Project work - Phase-II	100	100	200
8	Technical Seminar	100		
9	Co-curricular Activities	----	-----	Certificate from any agency

10. Evaluation Methodology – Distribution and Weightage of Marks:

A candidate shall be deemed to have secured the minimum academic requirement in a subject if he/she secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

10.1. Theory Courses:

a. Continuous Internal Evaluation (CIE):

i. There shall be five units in each of the theory subjects.
ii. For each theory course, during the semester, there shall be two CIEs. Each CIE will be evaluated for 40 marks. The first CIE will be conduct for around 50% [2.5 Units] of the syllabus and the second CIE will be conduct for the remaining 50% [2.5 Units] of the syllabus.
iii. The duration of CIE examination is 120 minutes (20 Minutes for Objective & 100 Minutes for Subjective).
    a. Question paper shall consist 6 questions. It shall contain two either or type questions from each unit. The student has to answer any one question from a unit.
    b. Student shall answer 3 questions (one question from a unit) in all.
    c. Each question carries equal marks of 10 marks.
    d. However, each question may have 2 or 3 sub questions.
    e. The evaluation for the each subjective midterm examination is totally 30 Marks.
    f. The first midterm will be conducted for around 50% of the syllabus and the rest of the midterm will be conducted for the remaining syllabus.
    g. Objective paper shall be set for maximum of 20 bits for 10 marks. The time duration for the objective paper is 20 minutes. There shall be online/ offline examination (TWO) conducted during the respective mid examinations by the college.
    h. If the student is absent for the CIE examination, no re-exam shall be conducted and marks for that examination shall be considered as zero.
iv. The internal assessment for theory subject during a semester is as given in Table 5.

Table 5: Continuous Internal Evaluation for Theory courses

Mid-term	Type	Final Evaluation	Marks
MID-I	Objective & Subjective Test	Final mid marks are evaluated as **(Max. of Mid-I & Mid-II) * 0.8 + (Min. of Mid-I & Mid-II) * 0.2**	40 M
MID-II	Objective & Subjective Test		

b. Semester End Examination (SEE):

The following pattern shall be followed in the Semester End Examination:

i. Question paper shall consist 10 questions. It shall contain two either/or type questions from each unit. The student has to answer any one question from a unit.
ii. Student shall answer 5 questions (one question from a unit) in all.

iii. Each question carries equal marks of 12 marks.
iv. However, each question may have sub questions.
v. A candidate has to secure a minimum of 50% of marks to be declared successful. If he/she fails to obtain the minimum marks, he/she has to reappear for the same during the supplementary examinations as and when conducted.
vi. There shall be online evaluation for semester theory end examinations. The evaluation is completely online. A minimum of 50% of theory courses shall be sent for online external evaluation. Remaining courses evaluation shall be done by online internal evaluation.

10.2. Practical Courses:

The performance of a student in each practical course shall be evaluated for maximum of 100 marks. The distribution shall be 40 marks for Continuous Internal Evaluation and 60 marks for the Semester End Examination.

a. Continuous Internal Evaluation (CIE):

The Continuous Internal Evaluation (CIE) for laboratory courses is based on the following parameters as given in Table 6.

Table 6: Laboratory/Practical Courses Internal Assessment

Parameter	**Marks**
Day to day work	10
Record	10
Internal Laboratory Examinations	20
Total Marks:	**40**

b. Semester End Examination:

i. For laboratory/practical courses, the semester end examination shall be evaluated by a committee consisting and the components for evaluation as given in Table 7.

Table 7: External Assessment for Laboratory/Practical/Skill Courses

External evaluation committee :	**Components**	**Marks**
1. External Examiner 2. Internal Examiner-I 3. Internal Examiner-II	Procedure / Algorithm	10
	Experimentation/Program Execution	25
	Result	10
	Viva Voce	15
	Total Marks:	**60**

ii. The Head of the Department shall appoint the internal examiners and External examiner shall be appointed by the principal from a panel contains three members submitted by the Head of the Department.

iii. A candidate has to secure a minimum of 50% of marks to be declared successful. If he/she fails to obtain the minimum marks, he/she has to reappear for the same during the supplementary examinations as and when conducted.

10.3 Mandatory Non-Credit Courses:

There shall be no semester end examination for Mandatory Non-Credit Course (Audit Courses) with zero credits. However, attendance shall be considered while calculating aggregate attendance and student shall be declared to have passed the audit course only when he/she secures 50% or more in the Continuous Internal Assessment.

The duration of CIE examination for non-credit course is 120 minutes and question paper pattern for CIE as follows,

i. Question paper shall consist 6 questions. It shall contain two either/or type questions from each unit. The student has to answer any one question from a unit.
ii. Student shall answer 3 questions (one question from a unit) in all.
iii. Each question carries equal marks of 10 marks.
iv. However, each question may have sub questions.
v. The evaluation for the each subjective midterm examination is totally 30 Marks.
vi. The first midterm will be conduct for around 50% of the syllabus and the rest of the midterm will be conduct for the remaining syllabus.
vii. If the student is absent for the CIE examination, no re-exam shall be conducted and marks for that examination shall be considered as zero.
viii. A candidate has to secure a minimum of 50% of marks to be declared successful. If he/she fails to obtain the minimum marks, he/she has to reappear for the same during the supplementary examinations as and when conducted.
ix. Final or consolidated CIE marks will be calculated by considering the marks secured by the student in both the CIEs with 80% weightage given to the better CIE and 20% to the other.

10.4. Industrial Internship:

i. Industrial Internship must involve practical work related to industry practices. A student shall undergo the internship either onsite or virtual along with Project Phase-2 for a period of 8 weeks, scheduled during IV semester.
ii. The student shall submit a technical report & Internship completed certificate for evaluation. This shall be evaluated at end of the IV semester for 100 marks by an Internship Review Committee (IRC).
iii. The IRC consists of Head of the department along with Supervisor andInternship Coordinator.
iv. The internal evaluation of the Internship as given in Table 8 and there shall be no SEE evaluation.

Table 8: Internal Assessment of Internship

Internship Review committee :	**Components**	**Marks**
1. Supervisor 2. Internship Coordinator 3. Head of the Department	Presentation	40
	Internship Report	60
	Total Marks :	**100**

v. The student must secure 50% or more marks for the total of 100 marks for getting the 2 credits.
vi. In case, if a student fails, he/she shall reappear as and when the IV semester supplementary examinations are scheduled.

10.5. Project work Phase-I & Phase-II:

The evaluation of the Project work is for 300 marks with 200 marks for internal evaluation and 100 marks for external evaluation. The Internal evaluation of 200 marks shall be done in Project work phase-I & phase-II.

a. Continuous Internal Evaluation (CIE):

i. A candidate is permitted to register for the Project Work in III Semester after satisfying the attendance requirement in all the subjects, both theory and laboratory (in I & II semesters) and continued in IV semester.
ii. Continuous assessment of Project Work phase-I and Project Work phase–II in III & IV semesters respectively will be monitored by the Project Review Committee (PRC).
iii. A candidate must present in Project Work Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PRC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PRC can the student initiate the project work.
iv. The internal evaluation of Project work phase-I for Review-II is 100 marks & 100 marks for project work phase-II for Review. The distribution of the marks for Continuous internal Assessment is given in the Table 9.

Table 9: Project work Internal Assessment

Project Review committee(PRC)	**Project Phase**	**Components**		**Division of Marks**	
1. Supervisor 2. Project Coordinator 3. Head of the Department	Phase-I	Review – I&II	PRC	50	100
			Supervisor	50	
	Phase-II	Review – III	PRC	50	100
			Supervisor	50	
			Total Marks:	**200**	

v. A candidate shall register the project work with the approval from the PRC, by giving presentation on project work to the PRC within four weeks from the commencement of III semester. After obtaining the approval of the PRC, the student shall initiate the project work.
vi. A candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PRC before submission of the Project dissertation.

vii. The Project work Review-II in III semester & Review-III in IV semester is evaluated by PRC for 100 marks for each review and PRC will examine the progress of the Project Work.

viii. A candidate to secure a minimum of 50% of marks in review-II & review-II assessed by PRC. The student fails to fulfil requirements, then must reappear the project review after two weeks.

b. Semester End Examination:

i. External evaluation of final Project work viva voce in IV semester shall be for 100 marks.

ii. Make any changes and incorporate the suggestions advised by the PRC Committee in dissertation and submit the same for plagiarism checking in Examination Section by paying stipulated fee. The candidate allows the similarity content less than 30%, if the candidate fails the requirement, then the dissertation is rejected for further proceedings.

iii. Research paper related to the Project Work shall be published in conference proceedings/UGC recognized journal. A copy of the published research paper shall be attached to the dissertation.

iv. The Project Viva voce examinations shall be conducted by a board consisting of the Project Coordinator, Head of the Department and the external examiner who has adjudicated the dissertation.

v. The External examiner shall be appointed by the Principal from a panel contains three members submitted by the Head of the Department.

vi. The Dissertation Evaluation (Viva voce) in IV semester is evaluated for external evaluation of 100 marks. The marks distribution of the end evaluation as follows by the Table 10.

Table 10: Project work External Assessment

Committee constituted by the Department	**Components**	**Marks**
1. External Examiner 2. Project Coordinator 3. Head of the Department	Viva-Voce	60
	Project Report	40
	Total Marks:	**100**

The candidate has to secure a minimum of 50% marks in Viva voce examination. If candidate fails to fulfill the requirements as specified, candidate will reappear for the Project Viva voce examination only after three months. In the reappeared examination also, if candidate fails to fulfill the requirements, candidate will not be eligible for the award of the degree.

10.6. Technical Seminar:

i. There shall be a Technical Seminar during II semester for internal evaluation of 100 marks.

ii. A student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Seminar Review Committee consisting of Head of the Department, supervisor/ mentor and two other faculty members of the department.

iii. The student has to secure a minimum of 50% of marks, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when supplementary examinations are conducted.

iv. The Technical seminar shall be conducted anytime during the semester as per the convenience of the Seminar Review Committee and students. There shall be **no SEE examination** for Technical Seminar.

10.7. Co-curricular Activities:

The college shall be introducing Co-Curricular activities in IV semester with TWO credits. The student must be participating in Co-Curricular / extra-curricular activities such as publishing a paper or participating in a National / International workshops / symposium / seminar / training organized by any private institution / Govt. organization / Training centers in virtual/offline mode. The student has to participate in Co-Curricular activities during their program duration and submit the certificate at the end of the IV semester. If he/she fails to submit will not be eligible for the award of degree. In such cases, the student shall repeat and submit the Co-Curricular activity.

The guidelines for awarding the credits to co-curricular activities are given in below table

S.No	Name of the Activity	Maximum Credits
1	Participation in the one week national level workshop/training programs	1.0
2	International workshops / training program Participation (Minimum of 6 days)	2.0
3	Participation in State level/National level Hackathon/seminar/conferences	1.0
4	Meritorious certificate in State level / National level Hackathon/Seminar /conferences	2.0
5	Participation in International Hackathons/seminar/conferences held outside India	2.0
6	Academic Award/Research Award from State level/National level Agencies	1.0
7	Academic Award/Research Award from International Agencies	2.0
8	Research /Review publications indexed in UGC Care list Journals	1.0
9	Research /Review publications indexed in Scopus/Web of Science Journals	2.0
10	Patent Filing	1.0

Note:

i). Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit.

ii). Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.

iii). Participation in any activity shall be permitted only once for acquiring required credits under Co-curricular activities.

10.8. Massive Open Online Courses (MOOCs):

1. There are six Elective Courses offered by Department/ discipline of the college during the program.
2. The student has to register at least any one elective course and complete the course through MOOCs for credit transfer and award the degree.
3. The student can enroll and complete the MOOC course(s) in advance.
4. The MOOCs offering agencies/ organizations must be approved by BOS.
5. The courses offered by the agencies/ organizations must be approved by Head of the department in consultation with the internal subject experts.
6. *A MOOC course, online assignment, programming assignment (if any) and proctor exam marks together taken as Final Marks (i.e.,100 marks) for that subject for credit transfer.*
7. The MOOCs offered by SWAYAM / other online platforms approved by BOS are registered for 12 weeks with the acceptance of Head of the Department. However, a student shall choose Elective course from the list in such a manner that he/she has not studied the same course in any form during the Program.
8. Attendance will not be monitored for MOOCs. Student has to pursue and acquire a certificate for MOOCs only from the organizations/agencies approved by the BOS in order to earn the credits for Elective courses.
9. The Head of the Department shall notify the list of such courses at the beginning of the semester. However, credits obtained through MOOCs will be shown against in the appropriate semester.
    i. The college shall invite registration forms from the students at the beginning of the semester for offering Program elective & open Elective courses. There shall be no limit on the minimum and maximum number of registrations based on class/ section strength. Examination fee, if any, will be borne by the student.
    ii. The student must complete ONE MOOCs for the award of M.Tech degree during their program. However, the pass certificate should be submitted in the appropriate semester for credit transfer. If students register for the courses through MOOCs and if he/she fails to complete this course, the college shall conduct offline examination during the same semester.
    iii. Students who have qualified in the proctored examinations conducted by the SWAYAM/ organization/ agency approved by the BOS can apply for credit transfer as specified are exempted from appearing internal as well as external examination (for the specified equivalent credit course only) conducted by the

college. The college level committee will allot equivalent marks/ grades/ credits based on the assessment certificate submitted.

10.9 Credit Transfer Policy:

As per University Grants Commission (Credit Framework for Online Learning Courses through any agency include SWAYAM) Regulation, 2016, the Institution shall allow up to 40% of the total courses being offered in a particular Programme in a semester through the Online Learning courses through online agencies including SWAYAM and the list approved by the BOS.

i. The College shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM/any agency platform.
ii. The online learning courses available on the SWAYAM/any agency platform will be considered for credit transfer. SWAYAM/any agency course credits are as specified in the platform.
iii. Student registration for the MOOCs shall be only through the institution, it will be mandatory for the student to share necessary information with the institution.
iv. The institution shall select the courses to be permitted for credit transfer through SWAYAM/any agency. However, while selecting courses in the online platform institution would essentially avoid the courses offered through the curriculum in the offline mode.
v. The institution shall notify at the beginning of semester the list of the online learning courses eligible for credit transfer in the forthcoming Semester.
vi. The institution shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester.
vii. The institution shall designate a faculty member as a Mentor for each course to guide the students from registration till completion of the credit course.
viii. The Institution shall ensure no overlap of SWAYAM/any agency MOOC exams with that of the Semester End Examination schedule. In case of delay in SWAYAM/ any agency results, the marks sheet will be re-issued for such students.
ix. Students pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the percentage of marks and grades.
x. It is permitted to register MOOCs courses in advance.
xi. The student has to submit the certificate of qualifying the MOOCS (through SWAYAM/ any agency) along with the undertaking form to consider that certificate for credit transfer.
xii. Once after submitting the undertaking form, the student shall not be permitted to write the same course again in MOOCs or as the regular course mode.
xiii. However, the student can write the examination as a regular course without submitting the undertaking form, by which he can finalise the option of submitting MOOCs certificate after the results are declared. In such case, the marks sheet of that particular student(s) will be re-issued.
xiv. The Department shall submit the following to the examination section of the Institution:

a. List of students who have passed MOOC courses related to a particular semester along with the certificates of completion.
b. Undertaking form filled by the students for credit transfer.

11. Re-registration for Improvement of Internal Evaluation Marks:

A candidate shall be given one chance to re-register for each theory subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination.

Following are the conditions for Re-Registration of Theory Courses for improvement of internal evaluation Marks:

i. In the duration of course work and obtained examinations results for I, II and III semesters.
ii. Out of the subjects the candidate has failed in the examination due to Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **THREE** Theory subjects for Improvement of Internal evaluation marks.
iii. The candidate has to re-register for the chosen subjects and fulfill the academic requirements.
iv. For each theory subject, the candidate has to pay the requisite fee along with the requisition through concerned Head of the department
v. In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

12. Transfer Rules:

There shall be no branch transfers after the completion of admission process.

13. Grading:

i. As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed,
ii. After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given in Table 11, depending on the range in which the marks obtained by the student fall.

Table 11: Structure of Grading of Academic Performance

Range in which % marks in the subject fall	Grade Assigned	Grade points
≥ 90	S (Superior)	10
≥ 80 < 90	A (Excellent)	9
≥ 70 < 80	B (Very Good)	8
≥ 60 < 70	C (Good)	7
≥ 50 < 60	D (Pass)	6
< 50	F (Fail)	0
Absent	Ab (Absent)	0

iii. A student obtaining Grade 'F' or Grade 'Ab' in a subject shall be considered failed and will be required to reappear for that subject when it is offered the next supplementary examination.

iv. For non-credit audit courses, "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage.

14. Computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

i. The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA = \left(\frac{\sum(C_i \, X \, G_i)}{\sum C_i}\right)$$

where, C_i is the number of credits of the ith subject and

G_i is the grade point scored by the student in the ith course.

ii. The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses undergone by a student over all the semesters of a program, i.e.,

$$CGPA = \left(\frac{\sum(C_i \, X \, S_i)}{\sum C_i}\right)$$

where "S_i" is the SGPA of the i^{th} semester and C_i is the total number of credits up to that semester.

iii. Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

iv. While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.

v. **Grade Point:** It is a numerical weight allotted to each letter grade on a 10-point scale.

vi. **Letter Grade:** It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D, F, Ab and MP (Malpractice).

vii. As per AICTE regulations, conversion of CGPA into equivalent percentage as follows:

Equivalent Percentage = (CGPA – 0.50) X 10

15. Award of Class:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes as presented in the Table 12.

Table 12: Award of Class

Class Awarded	Percentage of Marks to be secured
First Class with Distinction	≥70%
First Class	< 70% ≥ 60%
Pass Class	< 60% ≥ 50%

16. Exit Policy:

The student shall be permitted to exit with a PG Diploma based on his/her request to the university through the respective institution at the end of first year subject to passing all the courses in first year.

The University shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE and State government.

17. Withholding of Results:

The result of a candidate shall be withheld if:

a. He/she has not cleared any dues to the Institution/ Hostel/ University.
b. A case of disciplinary action against him/her is pending disposal.

18. Transitory Regulations

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfilment of academic regulations. Candidates who have been detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to Section 2 and they will follow the academic regulations into which they are readmitted.

19. Ragging:

Ragging of any kind is strictly prohibited. A Student who indulges in ragging shall be punished as per the provisions of the Ragging Act.

20. Amendment of Regulations:

The college may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the college.

21. General Instructions:

The academic regulations should be read as a whole for purpose of any interpretation.

a. Malpractices rules-nature and punishments are appended.
b. Where the words “he”, “him”, “his”, occur in the regulations, they also include “she”, “her”, “hers”, respectively.
c. In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

RULES FOR

DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The Hall Ticket of the candidate is to be cancelled and handed over to the examination of the autonomous college.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practical and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for four consecutive semesters from class work and all examinations, if his involvement is established. Otherwise, the candidate is debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject only.
6.	Refuses to obey the orders of the Chief Superintendent /Assistant - Superintendent /any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty inor outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the Controller of Examinations / Assistant Controller of Examinations, or anyperson on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. If the candidate physically assaults the invigilator/ Controller of Examinations / Assistant Controller of Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the policeand a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjectsthe candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjectsthe candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.

9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the college expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person (s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject only or in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations, depending on the recommendation of the committee.
12.	If any malpractice is detected, which is not covered inthe above clauses 1 to 11 shall be reported to the College for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved inencouraging malpractices)
3. A show cause notice shall be issued to the college.
4. Impose a suitable fine on the college.
5. Shifting the examination centre from the college to another college for a specific periodof not less than one year.

Note:-

Whenever the performance of a student is cancelled in any subject/subjects due to Malpractice, he has to register for End Examinations in that subject/subjects consequently and has to fulfil allthe norms required for the award of Degree.

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M.Tech I Semester
Course Structure

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem. - Course Structure

S.No	Subject Code	Course Category	Name of the Subject	Hours/Week				Marks		
				Lecture	Tutorial	Practical	Credits	Internal	External	Total
1	23D57101	PC	CMOS ANALOG IC DESIGN	3	0	0	3	40	60	100
2	23D57102	PC	CMOS DIGITAL IC DESIGN	3	0	0	3	40	60	100
3	23D57103	PE	MICROCHIP FABRICATION TECHNIQUES	3	0	0	3	40	60	100
4	23D57104	PE	NANOMATERIALS AND NANOTECHNOLOGY	3	0	0	3	40	60	100
5	23D57105	PE	CAD for VLSI	3	0	0	3	40	60	100
6	23D57106	PE	DEVICE MODELLING	3	0	0	3	40	60	100
7	23D57107	PE	FPGA ARCHITECTURES AND APPLICATIONS	3	0	0	3	40	60	100
8	23D57108	PE	ASIC DESIGN	3	0	0	3	40	60	100
9	23D57109	PC	CMOS ANALOG IC DESIGN LAB	0	0	4	2	40	60	100
10	23D57110	PC	CMOS DIGITAL IC DESIGN LAB	0	0	4	2	40	60	100
11	23D57111	MC(C)	RESEARCH METHODOLOGY AND IPR	2	0	0	2	40	60	100
12	23D57112	MC(NC)	ENGLISH FOR RESEARCH PAPER WRITING	2	0	0	0	40	0	40
13	23D57113	MC(NC)	DISASTER MANAGEMENT	2	0	0	0	40	0	40
14	23D57114	MC(NC)	SANSKRIT FOR TECHNICAL KNOWLEDGE	2	0	0	0	40	0	40

M.Tech I Semester Syllabus

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(23D57101) CMOS ANALOG IC DESIGN

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
2. Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
3. Intuitive understanding and real-life applications are emphasized throughout the course.
4. To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.
5. To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

UNIT-I BASIC MOS DEVICE PHYSICS

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage

UNIT-II FREQUENCY RESPONSE OF AMPLIFIERS

General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT-III FREQUENCY RESPONSE OF AMPLIFIERS

General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV FEEDBACK AMPLIFIERS

General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation

UNIT-V COMPARATORS

Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open□Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. 1. B.Razavi, “Design of Analog CMOS Integrated Circuits”,
2. 2 ndEdition, McGraw Hill Edition2016. 2. Paul.R.Gray& Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley, 5 thEdition, 2009.

REFERENCE BOOKS:

1. T.C.Carusone, D.A.Johns&K.Martin, “Analog Integrated Circuit Design”, 2 ndEdition, Wiley, 2012
2. P.E.Allen&D.R.Holberg, “CMOS Analog Circuit Design”, 3 rd Edition, Oxford University Press, 2011.
3. R.Jacob Baker, “CMOS Circuit Design, Layout, and Simulation”, 3 rdEdition, Wiley, 2010
4. Adel S. Sedra, Kenneth C. Smith, Arun, “Microelectronic Circuits”, 6 thEdition, Oxford University Press

COURSE OUTCOMES:

1. Design MOSFET based analog integrated circuits.
2. To Analyze Differential Amplifiers circuits.
3. To Understand Frequency Response of Amplifiers involved in analog integrated circuit design.
4. Understand and design the feedback amplifiers in analog circuits.
5. Understand and analyze the Characterization and performance of comparators

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(23D57102) CMOS DIGITAL IC DESIGN

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
2. The course also involves analysis of performance metrics.
3. To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
4. To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

UNIT-I MOS DESIGN PSEUDO NMOS LOGIC

Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic

UNIT-II COMBINATIONAL MOS LOGIC CIRCUITS

MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates

UNIT-III SEQUENTIAL MOS LOGIC CIRCUITS

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT-IV DYNAMIC LOGIC CIRCUITS

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V SEMICONDUCTOR MEMORIES

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4 th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3 rd Edition, 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

COURSE OUTCOMES:

1. Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS
2. Analyze, design and implement combinational MOS logic circuits.
3. Analyze, design and implement sequential MOS logic circuits.
4. To Understand the principle of dynamic logic circuits
5. Classify different semiconductor memories

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(23D57103) MICROCHIP FABRICATION TECHNIQUES

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. Comprehend impact of semiconductor industry on the design of development of integrated circuits.
2. Acquaint with clean room technology
3. Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
4. Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and 45nm technologies
5. Understand packaging principles

UNIT-I INTRODUCTION TO PROCESSING

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction

UNIT-II PHOTOLITHOGRAPHY

Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT-III DIFFUSION & ION IMPLANTATION

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT-IV FILM DEPOSITIONS AND GROWTH

Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

SANTHIRAM ENGINEERING COLLEGE

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V YIELD

Design rules and Scaling, BICMOS ICs:
Choice of transistor types, PNP transistors, Resistors, capacitors. Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997
2. Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall, 2000.

REFERENCE BOOKS:

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

COURSE OUTCOMES:

1. Understand various stages of fabrication
2. Understand various packaging techniques and Design rules
3. Understand the aspects of diffusion, ion implantation techniques.
4. Classify various thin films and its characteristics.
5. Specify NMOS and CMOS design rules corresponding to package operations.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(23D57105) CAD FOR VLSI

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
2. To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
3. To practice the application of fundamentals of VLSI technologies
4. To optimize the implemented design for area, timing and power by applying suitable constraints.

UNIT-I INTRODUCTION

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II PARTITIONING

Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing

UNIT-III FLOOR PLANNING

Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT-IV PLACEMENT AND ROUTING & GLOBAL ROUTING AND DETAILED ROUTING

Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.
Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V PHYSICAL DESIGN AUTOMATION OF FPGAS AND MCMS

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3 rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

COURSE OUTCOMES:

1. Establish comprehensive understanding of the various phases of CAD for digital electronic systems.
2. Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement
3. Optimize the implemented design for area, timing and power by applying suitable constraints.
4. Practice the application of fundamentals of VLSI technologies
5. Gain knowledge on the methodologies involved in design, verification and implementation of digital designs on MCMs.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(23D57104) NANOMATERIALS AND NANOTECHNOLOGY

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the basic idea behind the design and fabrication of nano scale systems.
2. To understand and formulate new engineering solutions for current problems and technologiesfor future applications.
3. To acquire knowledge on the operation of fabrication and characterization devices to achieve precisely designed systems.

UNIT-I INTRODUCTION OF NANO MATERIALS AND NANOTECHNOLOGIES

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive–hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT-II FUNDAMENTALS OF NANOMATERIALS

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials. Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low Dimensional Carbon-Related Nanomaterials.

UNIT-III MICRO- AND NANOLITHOGRAPHY TECHNIQUES

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT-IV INTRODUCTION & SYNTHESIS OF CNTS - ARC-DISCHARGE

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT‟s - Multi-walled nanotubes, Single-walled nano tubes Optical properties of CNT‟s, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNTs

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V FERROELECTRIC MATERIALS

Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane based application, polymer based application

TEXT BOOKS:

1. Kenneth J.Klabunde and Ryan M.Richards, “Nanoscale Materials in Chemistry”, 2ndedition, John Wiley and Sons, 2009.
2. I Gusev and A Rempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1stIndian edition by Viva Books Pvt. Ltd. 2008.
3. B.S.Murty,P.Shankar,Baldev Raj, B.B.Rath, James Murday, “Nanoscience and Nanotechnology”, Tata McGrawHill Education 2012.

REFERENCE BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011
2. Digital Integrated Circuits - A Design Perspective, Jan M.Rabaey, AnantChandrakasan, Borvivoje Nikolic, 2nd Edition, PHI

COURSE OUTCOMES:

1. Understand the basic science behind the design and fabrication of nano scale systems.
2. Understand and formulate new engineering solutions for current problems and competing technologies for future applications.
3. To Understand the advantages and Challenges of MEMS
4. To analyze the synthesis of CNTs with applications.
5. To acquire knowledge on the operation and characterization to achieve precisely designed systems

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(23D57105) CAD FOR VLSI

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
2. To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
3. To practice the application of fundamentals of VLSI technologies
4. To optimize the implemented design for area, timing and power by applying suitable constraints.

UNIT-I INTRODUCTION

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II PARTITIONING

Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing

UNIT-III FLOOR PLANNING

Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT-IV PLACEMENT AND ROUTING & GLOBAL ROUTING AND DETAILED ROUTING

Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.
Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V PHYSICAL DESIGN AUTOMATION OF FPGAS AND MCMS

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3 rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

COURSE OUTCOMES:

1. Establish comprehensive understanding of the various phases of CAD for digital electronic systems.
2. Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement
3. Optimize the implemented design for area, timing and power by applying suitable constraints.
4. Practice the application of fundamentals of VLSI technologies
5. Gain knowledge on the methodologies involved in design, verification and implementation of digital designs on MCMs.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(23D57106) DEVICE MODELLING

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the physics of 2-terminal MOS operation and its characteristics
2. To understand the physics of 4-terminal MOSFET operation and its characteristics.
3. To analyze the SOI MOSFET electrical characteristics.

UNIT-I 2-TERMINAL MOS DEVICE

Threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT-II C-V CHARACTERISTICS

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit);MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit)

UNIT-III 4-TERMINAL MOSFET

Threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT-IV SUB THRESHOLD CURRENT MODELS

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer‟s model)

UNIT-V SOI MOSFET

Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

TEXT BOOKS:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

REFERENCE BOOKS:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995
3. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009

COURSE OUTCOMES:

1. Understand the physics of 2-terminal MOS operation and its characteristics
2. Understand the concept of MOScapacitor.
3. Understand the physics of 4-terminal MOSFET operation and its characteristics.
4. To understand Sub threshold current model.
5. Analyze the SOI MOSFET electrical characteristics

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(23D57107) FPGA ARCHITECTURES AND APPLICATIONS

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To acquire knowledge about various architectures and device technologies of PLD‟s.
2. To comprehend FPGA Architectures
3. To analyze System level Design and their application for Combinational and Sequential Circuits.
4. To familiarize with Anti-Fuse Programmed FPGAs.
5. To apply knowledge of this subject for various design applications.

UNIT-I INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation

UNIT-II FIELD PROGRAMMABLE GATE ARRAYS

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT-III SRAM PROGRAMMABLE FPGA

Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT-IV ANTI-FUSE PROGRAMMED FPGAS

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures

UNIT-V DESIGN APPLICATIONS

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

SANTHIRAM ENGINEERING COLLEGE

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning

REFERENCE BOOKS:

1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier, Newnes
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series

COURSE OUTCOMES:

1. Acquire knowledge about various architectures and device technologies of PLD‟s
2. Comprehend FPGA Architectures
3. Analyze System level Design and their applications for various architectures.
4. Familiarize with Anti-Fuse Programmed FPGAs
5. Apply knowledge of this subject for various design applications.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
3	0	0	3

(23D57108) ASIC DESIGN

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand different types of ASICs and their libraries.
2. To understand about programmable ASICs, I/O modules and their interconnects.
3. To familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT-I INTRODUCTION TO ASICS

Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design

UNIT-II PROGRAMMABLE ASICS AND PROGRAMMABLE ASIC LOGIC CELLS

The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT-III I/O CELLS AND INTERCONNECTS & PROGRAMMABLE ASIC DESIGN SOFTWARE

DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT-IV LOW LEVEL DESIGN ENTRY AND LOGIC SYNTHESIS

Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V SIMULATION, TEST AND ASIC CONSTRUCTION

Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

TEXT BOOKS:

1. Michael John Sebastian Smith, “Application Specific Integrated Circuits”, Pearson Education, 2003.
2. L.J.Herbst, “Integrated Circuit Engineering”, Oxford Science Publications, 1996.

REFERENCE BOOKS:

1. HimanshuBhatnagar, “Advanced ASIC Chip Synthesis using Synopsis Design Compiler”, 2nd Edition, Kluwer Academic, 2001

COURSE OUTCOMES:

1. Understand different types of ASICs and their libraries.
2. Understand about programmable ASICs, I/O modules and their interconnects.
3. Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.
4. Understand the various Low Level Design Entry and Logic Synthesis
5. Analyze and Simulate the various Tests and ASIC Construction.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
0	0	4	2

(23D57109) CMOS ANALOG IC DESIGN LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To explain the VLSI Design Methodologies using VLSI design tool.
2. To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. To explain the Physical Verification in Layout Design
4. To fully appreciate the design and analyze of analog and mixed signal simulation
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

The students are required to design and implement any **TEN** Experiments using CMOS 130nm Technology.

The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:

Software: Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator

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(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

Hardware: Personal Computer with necessary peripherals, configuration and operating System.

COURSE OUTCOMES:

1. Explain the VLSI Design Methodologies using VLSI design tool.
2. Grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. Explain the Physical Verification in Layout Design
4. Fully appreciate the design and analyze of analog and mixed signal simulation
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
0	0	4	2

(23D57110) CMOS DIGITAL IC DESIGN LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To explain the VLSI Design Methodologies using any VLSI design tool.
2. To grasp the significance of various design logic Circuits in full-custom IC Design.
3. To explain the Physical Verification in Layout Extraction.
4. To fully appreciate the design and analyze of CMOS Digital Circuits.
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

The students are required to design and implement the Circuit and Layout of any **TEN** Experiments using CMOS 130nm Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software: Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware: Personal Computer with necessary peripherals, configuration and operating System

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

COURSE OUTCOMES:

1. Explain the VLSI Design Methodologies using any VLSI design tool
2. Grasp the significance of various design logic Circuits in full-custom IC Design.
3. Explain the Physical Verification in Layout Extraction
4. Fully appreciate the design and analyze of CMOS Digital Circuits
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

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(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	2

(23D57111) RESEARCH METHODOLOGY AND IPR

Course Category	Mandatory Course (credit)
Course Enrichment Relevance	Professional Ethics

COURSE OBJECTIVES:

1. Identify an appropriate research problem in their interesting domain.
2. Understand ethical issues understand the Preparation of a research project thesis report.
3. Understand the Preparation of a research project thesis report
4. Understand the law of patent and copyrights.
5. Understand the Adequate knowledge on IPR

UNIT-I RESEARCH PROBLEMS

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary Instrumentations

UNIT-II EFFECTIVE LITERATURE STUDIES APPROACHES

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT-III NATURE OF INTELLECTUAL PROPERTY

Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-IV PATENT RIGHTS

Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT-V NEW DEVELOPMENTS IN IPR

Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science & engineering students‟
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”
2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007”
3. Mayall, “Industrial Design”, McGraw Hill, 1992
4. Niebel, “Product Design”, McGraw Hill, 1974
5. Asimov, “Introduction to Design”, Prentice Hall, 1962
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “ Intellectual Property in New Technological Age”, 2016.

COURSE OUTCOMES:

1. Analyze research related information
2. Follow research ethics
3. Understand that today‟s world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
4. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular
5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(23D57112) ENGLISH FOR RESEARCH PAPER WRITING

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Skill Development**

COURSE OBJECTIVES:

1. Understand the essentials of writing skills and their level of readability
2. Learn about what to write in each section
3. Ensure qualitative presentation with linguistic accuracy

UNIT-I OVERVIEW OF A RESEARCH PAPER

Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breaking up Long Sentences-Structuring Paragraphs and Sentences-Being Concise and Removing Redundancy -Avoiding Ambiguity

UNIT-II ESSENTIAL COMPONENTS OF A RESEARCH PAPER

Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Cauterization

UNIT-III INTRODUCING REVIEW OF THE LITERATURE

Introducing Review of the Literature ??? Methodology - Analysis of the Data-Findings - Discussion-Conclusions-Recommendations.

UNIT-IV SKILLS FOR WRITING PAPER

Key skills needed for writing a Title, Abstract, and Introduction

UNIT-V APPROPRIATE LANGUAGE TO FORMULATE METHODOLOGY

Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions

TEXT BOOKS:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books) Model Curriculum of Engineering & Technology PG Courses [Volume-I]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman‟sbook

4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

COURSE OUTCOMES:

1. Understand the significance of writing skills and the level of readability
2. Analyze and write title, abstract, different sections in research paper
3. Develop the skills needed while writing a research paper

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(23D57113) DISASTER MANAGEMENT

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Human Values**

COURSE OBJECTIVES:

1. Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response
2. Critically evaluate disaster risk reduction and humanitarian response policy and practice from Multiple perspectives
3. Develop and understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations
4. Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in

UNIT-I INTRODUCTION & DISASTER PRONE AREAS IN INDIA

Disaster:Definition,FactorsandSignificance;DifferenceBetweenHazardandDisaster;Naturaland Manmade Disasters: Difference, Nature, Types and Magnitude.
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II REPERCUSSIONS OF DISASTERS AND HAZARDS

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes,Volcanisms,Cyclones,Tsunamis,Floods,Droughts and Famines,Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdow

UNIT-III DISASTER PREPAREDNESS AND MANAGEMENT

Preparedness: Monitoring of Phenomena Triggering ADisasteror Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness

UNIT-IV RISK ASSESSMENT DISASTER RISK

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. TechniquesofRiskAssessment,GlobalCo-OperationinRiskAssessmentand Warning, People???s Participation in Risk Assessment. Strategies for Survival.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V DISASTER MITIGATION

Meaning,ConceptandStrategiesofDisasterMitigation,EmergingTrendsInMitigation.Structural Mitigationand Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS:

1. R.Nishith,SinghAK,DisasterManagementinIndia:Perspectives,issuesandstrategies
2. New Royal book Company.Sahni, PardeepEt.Al.(Eds.), Disaster Mitigation Experiences And Reflections, Prentice Hall Of India, New Delhi.
3. GoelS.L.,DisasterAdministrationAndManagementTextAndCaseStudies,Deep&Deep Publication Pvt. Ltd., New Delhi

COURSE OUTCOMES:

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(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. I Sem.

L	T	P	C
2	0	0	0

(23D57114) SANSKRIT FOR TECHNICAL KNOWLEDGE

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Skill Development**

COURSE OBJECTIVES:

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning
3. Learning of Sanskrit to develop the logic in mathematics, science &other subjects enhancing the memory power
4. The engineering scholars equipped with Sanskrit will be able to explore the huge
5. Knowledge from ancient literature

UNIT-I INTRODUCTION

Alphabets in Sanskrit

UNIT-II SENTENCES

Past/Present/Future Tense, Simple Sentences

UNIT-III INTRODUCTION OF ROOTS

Order, Introduction of roots

UNIT-IV LITERATURE ABOUT SANSKRIT

Technical information about Sanskrit Literature

UNIT-V TECHNICAL CONCEPTS OF ENGINEERING

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS:

1. “Abhyaspustakam” –Dr.Vishwas, Sanskrit-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Prathama Deeksha- Vempati Kutumbshastri, RashtriyaSanskrit Sansthanam, New Delhi Publication
3. “India‟s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd.,New Delhi

COURSE OUTCOMES:

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

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1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science &technology can be understood
3. Being a logical language will help to develop logic in students

M.Tech II Semester Course Structure

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem. - Course Structure

S.No	Subject Code	Course Category	Name of the Subject	Hours/Week				Marks		
				Lecture	Tutorial	Practical	Credits	Internal	External	Total
1	23D57201	PC	CMOS MIXED SIGNAL IC DESIGN	3	0	0	3	40	60	100
2	23D57202	PC	PHYSICAL DESIGN AUTOMATION	3	0	0	3	40	60	100
3	23D57203	PE	SOC TESTING AND VERIFICATION	3	0	0	3	40	60	100
4	23D57204	PE	SEMICONDUCTOR MEMORY DESIGN AND TESTING	3	0	0	3	40	60	100
5	23D57205	PE	MEMS SYSTEM DESIGN	3	0	0	3	40	60	100
6	23D57206	PE	LOW POWER VLSI DESIGN	3	0	0	3	40	60	100
7	23D57207	PE	IOT AND ITS APPLICATIONS	3	0	0	3	40	60	100
8	23D57208	PE	VLSI SIGNAL PROCESSING	3	0	0	3	40	60	100
9	23D57209	PC	CMOS MIXED SIGNAL IC DESIGN LAB	0	0	4	2	40	60	100
10	23D57210	PC	PHYSICAL DESIGN AUTOMATION LAB	0	0	4	2	40	60	100
11	23D57212	MC(NC)	PEDAGOGY STUDIES	2	0	0	0	40	0	40
12	23D57213	MC(NC)	STRESS MANAGEMENT FOR YOGA	2	0	0	0	40	0	40
13	23D57214	MC(NC)	PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS	2	0	0	0	40	0	40

M.Tech II Semester Syllabus

SANTHIRAM ENGINEERING COLLEGE

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(23D57201) CMOS MIXED SIGNAL IC DESIGN

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To demonstrate first order filter with least interference
2. To extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
3. To design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT-I SWITCHED CAPACITOR CIRCUITS

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters

UNIT-II PHASED LOCK LOOP (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III DATA CONVERTER

Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT-IV A TO D CONVERTERS

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Sigma Delta A/D converters, Time- interleaved converters.

UNIT-V OVERSAMPLING CONVERTERS

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A

TEXT BOOKS:

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

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1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002 2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inter science, 2005. 3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009

COURSE OUTCOMES:

1. To understand, analyze and design Switched capacitor filter circuits
2. To analyze and design the PLL circuits.
3. To analyze and design the different D/A converters.
4. To analyze and design the different A/D converters.
5. To analyze modulators, filters and converters

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(23D57202) PHYSICAL DESIGN AUTOMATION

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand relation between automation algorithms and constraints posed by VLSI technology.
2. To adopt algorithms to meet critical design parameters.
3. To design area efficient logics by employing different routing algorithms and shape functions.
4. To simulate and synthesis different combinational and sequential logics.

UNIT-I VLSI DESIGN AUTOMATION TOOLS

Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT-II LAYOUT

Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT-III FLOOR PLANNING AND ROUTING

Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT-IV SIMULATION AND LOGIC SYNTHESIS

Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis.

UNIT-V HIGH-LEVEL SYNTHESIS

Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

TEXT BOOKS:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998

2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999

REFERENCE BOOKS:

1. S.M. Sait,H.Youssef, VLSI Physical Design Automation, World scientific, 1999
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

COURSE OUTCOMES:

1. To understand the various VLSI design flows and applications in the VLSI technology.
2. To remember the design rules and apply in the VLSI design verification process.
3. To understand and apply routing and placement algorithms to meet critical design parameters.
4. To evaluate the VLSI design for logical synthesis using simulation tools.
5. To apply various synthesis models for the different combinational and sequential circuits.

SANTHIRAM ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(23D57203) SOC TESTING AND VERIFICATION

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the concepts of faults and testing in SoC
2. To implement the faults using simulation tools
3. To analyze BIST systems

UNIT-I INTRODUCTION TO TESTING

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II LOGIC AND FAULT SIMULATION

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation

UNIT-III TESTABILITY MEASURES

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV BUILT-IN SELF-TEST

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V BOUNDARY SCAN STANDARD

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. M.L. Bushnell, V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Kluwer Academic Pulishers

2. M. Abramovici, M.A.Breuer and A.D Friedman, Digital Systems and Testable Design, Jaico Publishing House.

REFERENCE BOOKS:

1. P.K. Lala, Digital Circuits Testing and Testability, Academic Press

COURSE OUTCOMES:

1. To understand the types faults and the concepts of faults and testing in SoC
2. To understand the algorithms to detect the faults using simulation tools.
3. To understand and apply the concepts of observability and controllability.
4. To apply and evaluate the circuit under test using BIST
5. To apply and evaluate the circuit under test using Boundary Scan tests.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(23D57204) SEMICONDUCTOR MEMORY DESIGN AND TESTING

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand different types of memories, their architectural and different packing techniques of memories.
2. To build fault models for memory testing
3. To analyze different parameters that lead malfunctioning of memories
4. To design reliable memories with efficient architecture to improve processes times and power.

UNIT-I RANDOM ACCESS MEMORY TECHNOLOGIES

SRAM: SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II NON-VOLATILE MEMORIES

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT-III MEMORY FAULT MODELING TESTING AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE

RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

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UNIT-IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures.

UNIT-V ADVANCED MEMORY TECHNOLOGIES AND HIGH-DENSITY MEMORY PACKING TECHNOLOGIES

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXT BOOKS:

1. Semiconductor Memories Technology Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories Architecture, Design and Applications - Ashok K. Sharma, 2002, Wiley.

REFERENCE BOOKS:

1. Modern Semiconductor Devices for Integrated Circuits Chenming C Hu, First Edition. Prentice all

COURSE OUTCOMES:

1. To understand and analyze the SRAM and DRAM cell structures
2. To understand, remember and apply different types of memory cells in suitable applications.
3. To analyze and evaluate fault models for memory testing
4. To analyze the memories for reliability and radiation effects
5. To understand and remember advanced manufacturing technologies in memory cell designs.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(23D57205) MEMS SYSTEM DESIGN

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the basic concepts of MEMS technology and working of MEMS devices.
2. To understand and select different materials for current MEMS devices and competing technologies for future applications.
3. To understand the concepts of fabrication process of MEMS, Design and Packaging Methodology.
4. To analyze the various fabrication techniques in the manufacturing of MEMS Devices.

UNIT-I INTRODUCTION TO MEMS

Introduction to MEMS & Real-world Sensor/Actuator examples (DMD, Airbag, pressure sensors). MEMS Sensors in Internet of Things (IoT), Bio-Medical Applications

UNIT-II MEMS MATERIALS AND THEIR PROPERTIES

Materials (eg. Si, SiO2, SiN, Cr, Au, Ti, SU8, PMMA, Pt); Important properties: Young modulus, Poisson ratio, density, piezo-resistive coefficients, TCR, Thermal Conductivity, Material Structure. Understanding Selection of materials based on applications.

UNIT-III MEMS FAB PROCESSES-1

Understanding MEMS Processes & Process parameters for: Cleaning, Growth &Deposition, Ion Implantation & Diffusion, Annealing, Lithography. Understanding selection of Fab processes based on Applications.

UNIT-IV MEMS FAB PROCESSES-2

Understanding MEMS Processes & Process parameters for: Wet & Dry etching, Bulk& Surface Micromachining, Die, Wire& Wafer Bonding, Dicing, Packaging. Understanding selection of Fab processes based on Applications.

UNIT-V MEMS DEVICES

Architecture, working and basic quantitative behavior of Cantilevers, Micro heaters, Accelerometers, Pressure Sensors, Micro mirrors in DMD, Inkjet printer-head. Understanding steps involved in Fabricating above devices.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. An Introduction to Micro electromechanical Systems Engineering; 2nd Edition by N.Maluf, K Williams; Publisher: Artech House Inc
2. Practical MEMS - by Ville Kaajakari; Publisher: Small Gear Publishing
3. Micro system Design - by S. Senturia; Publisher: Springer

REFERENCE BOOKS:

1. Analysis and Design Principles of MEMS Devices Minhang Bao; Publisher: Elsevier Science
2. Fundamentals of Micro fabrication - by M. Madou; Publisher:CRC Press; 2ndedition
3. Micro Electro Mechanical System Design - by J. Allen; Publisher: CRC Press
4. Micro machined Transducers Sourcebook - by G. Kovacs; Publisher: McGraw-Hill

COURSE OUTCOMES:

1. To understand the basic concepts of MEMS technology and working of MEMS devices.
2. To understand and select different materials for current MEMS devices and competing technologies for future applications.
3. To understand the concepts of fabrication process of MEMS
4. To understand the concepts of fabrication process Design and Packaging Methodology of MEMS.
5. Analyze the various fabrication techniques in the manufacturing of MEMS Devices.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(23D57206) LOW POWER VLSI DESIGN

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
2. To implement Low power design approaches for system level and circuit level measures.
3. To design low power adders, multipliers and memories for efficient design of systems.

UNIT-I FUNDAMENTALS

Need for Low Power Circuit Design, Sources of Power Dissipation Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-II LOW-POWER DESIGN APPROACHES

Low-Power Design through Voltage Scaling VTCMOS circuits, MTCMOS circuits, Architectural Level Approach Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT-III LOW-VOLTAGE LOW-POWER ADDERS

Introduction, Standard Adder Cells, CMOS Adders Architectures. Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques. Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT-IV LOW-VOLTAGE LOW-POWER MULTIPLIERS

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-V LOW-VOLTAGE LOW-POWER MEMORIES

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits Analysis and Design Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

COURSE OUTCOMES:

1. To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect.
2. To design Low power design approaches for system level and circuit level measures.
3. To design and evaluate low power adders for efficient design of systems.
4. To design and evaluate low power multipliers for efficient design of systems.
5. To design and evaluate low power memories for efficient design of systems.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(23D57207) IOT AND ITS APPLICATIONS

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To apply the Knowledge in IOT Technologies and Data management.
2. To determine the values chains Perspective of M2M to IOT.
3. To implement the state of the Architecture of an IOT.
4. To compare IOT Applications in Industrial & real world.
5. To demonstrate knowledge and understand the security and ethical issues of an IOT.

UNIT-I FUNDAMENTALS OF IOT

Evolution of Internet of Things, Enabling Technologies, IoT Architectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.
IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT-II IOT PROTOCOLS

IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT-III DESIGN AND DEVELOPMENT

Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

UNIT-IV DATA ANALYTICS AND SUPPORTING SERVICES

Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT-V CASE STUDIES/INDUSTRIAL APPLICATIONS

IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)

TEXT BOOKS:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.
2. Internet of Things A hands-on approach, ArshdeepBahga, Vijay Madisetti, Universities Press,2015

REFERENCE BOOKS:

1. The Internet of Things Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
2. From Machine-to-Machine to the Internet of Things Introduction to a New Age of Intelligence, Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.

COURSE OUTCOMES:

1. To apply the Knowledge in IOT Technologies and Data management.
2. To determine the values chains Perspective of M2M to IOT.
3. To implement the state of the Architecture of an IOT.
4. Compare IOT Applications in Industrial & real world.
5. Demonstrate knowledge and understand the security and ethical issues of an IOT.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
3	0	0	3

(23D57208) VLSI SIGNAL PROCESSING

Course Category	**Professional Elective (PE)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To study the existing architectures suitable for VLSI.
2. To understand the concepts of folding and unfolding algorithms and applications.
3. To design new architectures suitable for VLSI.
4. To implement fast convolution algorithms.

UNIT-I INTRODUCTION TO DSP

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT-II FOLDING AND UNFOLDING

Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT-III SYSTOLIC ARCHITECTURE DESIGN

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT-IV FAST CONVOLUTION

Introduction Cook - Toom Algorithm Winogard algorithm Iterated Convolution Cyclic Convolution Design of Fast Convolution algorithm by Inspection.

UNIT-V LOW POWER DESIGN

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipelines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches.

SANTHIRAM ENGINEERING COLLEGE

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

TEXT BOOKS:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science, 1998
2. Kung S. Y, H. J. While House, T. Kailath ,VLSI and Modern Signal processing , Prentice Hall, 1985

REFERENCE BOOKS:

1. Jose E. France, Yannis Tsividis, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing , Prentice Hall, 1994
2. Medisetti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), 1995

COURSE OUTCOMES:

1. To study the existing architectures suitable for VLSI.
2. To understand the concepts of folding and unfolding algorithms and applications.
3. To design new architectures suitable for VLSI.
4. To implement fast convolution algorithms.
5. To apply low power approaches in the VLSI design for the signal processing.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
0	0	4	2

(23D57209) CMOS MIXED SIGNAL IC DESIGN LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To design and simulate op-amp for given specifications.
2. To design and simulate data converter for given specifications.
3. To design and simulate PLL and VCO for given specifications.
4. To understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

The students are required to design and implement the Circuit and Layout of the following.

Experiments using CMOS 130nm Technology.

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation

2) High speed comparator design

a. Two stage cross coupled clamped comparator.

b. Strobed Flip-flop

3) Data converter

Cycle 2:

1) Switched capacitor circuits

a. Parasitic sensitive integrator

b. Parasitic insensitive integrator

2) Design of PLL

3) Design of VCO

4) Band gap reference circuit

5) Layouts of All the circuits Designed and Simulated

Software:

Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

REFERENCE BOOKS:

1. David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2. R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley,1986.
3. Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4. Alan Hastlings, The art of Analog Layout, Wiley, 2005.

COURSE OUTCOMES:

1. Design and simulate op-amp for given specifications
2. Design and simulate data converter for given specifications
3. Design and simulate switched capacitor filters
4. Design and simulate PLL and VCO for given specifications
5. Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

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DEPARTMENT OF ECE - VLSI SYSTEM DESIGN

M.Tech. II Sem.

L	T	P	C
0	0	4	2

(23D57210) PHYSICAL DESIGN AUTOMATION LAB

Course Category	**Professional Core course (PC)**
Course Enrichment Relevance	**Employability**

COURSE OBJECTIVES:

1. To learn the implementation of different Physical Design Automation algorithms
2. To implement different graph algorithms
3. To implement different partitioning algorithms
4. To implement different floor planning algorithms
5. To implement different routing algorithms

Cycle 1:

1) Graph algorithms

a) Graph search algorithms

i. Depth first search

ii. Breadth first search

b) Spanning tree algorithm

i. Kruskals algorithm

c) Shortest path algorithm

i. Dijkstra algorithm

ii. Floyd- Warshall algorithm

d) Steiner tree algorithm

2) Computational geometry algorithm

a) Line sweep method

b) Extended line sweep method

Cycle 2:

3) Partitioning algorithms

a) Group migration algorithms

I. Kernighan Lin algorithm

II. Extensions of Kernighan-Lin algorithm

i) Fiduccias Mattheyses algorithm

ii) Goldberg and Burstein algorithm

b) Simulated annealing and evolution algorithms

i. Simulated annealing algorithm

ii. Simulated evolution algorithm

III) Metric allocation method

4) Floor planning algorithms

i) Constraint based methods

ii) Integer programming based methods

iii) Rectangular dualization based methods

iv) Hierarchical tree based methods

v) Simulated evolution algorithms

vi) Time driven Floor planning algorithms

5) Routing algorithms

I) Two terminal algorithms

a) Maze routing algorithms

i)Lees algorithm

ii) Soukups algorithm

iii) Hadlock algorithm

b) Line-Probe algorithm

c) Shortest path based algorithm

II) Multi terminal algorithm

a) Stenier tree based algorithm

i) SMST algorithm

ii) Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

TEXT BOOKS:

1. Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2. Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.

COURSE OUTCOMES:

1. Learn the implementation of different Physical Design Automation algorithms
2. Implement different graph algorithms
3. Implement different partitioning algorithms
4. Implement different floor planning algorithms
5. Implement different routing algorithms

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M.Tech. II Sem.

L	T	P	C
2	0	0	0

(23D57212) PEDAGOGY STUDIES

Course Category	Mandatory Course (Non-credit)
Course Enrichment Relevance	Skill Development

COURSE OBJECTIVES:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

UNIT-I INTRODUCTION AND METHODOLOGY

Aims and rationale, Policy back ground, Conceptual frame work and terminology Theories of learning,Curriculum,Teachereducation.Conceptual framework,Research questions. Overview of methodology and Searching.

UNIT-II THEMATIC OVERVIEW

Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT-III EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES, METHODOLOGY FOR THE IN DEPTH STAGE

Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the echo curriculum and guidance materials best support effective pedagogy. Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV PROFESSIONAL DEVELOPMENT

Alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment,Barriers to learning: limited resources and large class sizes

UNIT-V RESEARCH GAPS AND FUTURE DIRECTIONS

Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

REFERENCE BOOKS:

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1. AckersJ, HardmanF(2001)Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. AgrawalM(2004)Curricular reform in schools: The importance of evaluation, Journal of
3. Curriculum Studies, 36 (3): 361-379.
4. AkyeampongK(2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
5. Akyeampong K, LussierK, PryorJ, Westbrook J (2013)Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count International Journal Educational Development, 33 (3): 272282.
6. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell. Chavan M (2003)Read India: A mass scale, rapid, learning to read campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

COURSE OUTCOMES:

1. What pedagogical practices are being used by teachers informal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

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M.Tech. II Sem.

L	T	P	C
2	0	0	0

(23D57213) STRESS MANAGEMENT FOR YOGA

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Human Values**

COURSE OBJECTIVES:

1. To achieve overall health of body and mind
2. To overcome stress

UNIT-I DEFINITIONS OF EIGHT PARTS OF YOG.(ASHTANGA)

Definitions of Eight parts of yog.(Ashtanga)

UNIT-II YAM AND NIYAM.

Yam and Niyam.

UNIT-III DO S AND DONT S IN LIFE.

i) Ahinsa,satya,astheya,bramhacharya and aparigrahaii) Shaucha,santosh,tapa,swadhyay,ishwarpranidhan

UNIT-IV ASAN AND PRANAYAM

Asan and Pranayam

UNIT-V VARIOUS YOG POSES AND THEIR BENEFITS FOR MIND &BODY

i) Various yog poses and their benefits for mind &body
ii)Regularization of breathing techniques and its effects-Types of pranayam

REFERENCE BOOKS:

1. Yogic Asanas for Group Training-Part-I: Janardan Swami Yoga bhyasiMandal, Nagpur
2. Rajayogaor conquering the Internal Nature by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

COURSE OUTCOMES:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

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M.Tech. II Sem.

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2	0	0	0

(23D57214) PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

Course Category	**Mandatory Course (Non-credit)**
Course Enrichment Relevance	**Human Values**

COURSE OBJECTIVES:

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students

UNIT-I NEETISATAKAM- HOLISTIC DEVELOPMENT OF PERSONALITY

Verses-19,20,21,22(wisdom)
Verses-29,31,32(pride &heroism)
Verses-26,28,63,65(virtue)

UNIT-II NEETISATAKAM- HOLISTIC DEVELOPMENT OF PERSONALITY

Verses-52,53,59(dont s)
Verses-71,73,75,78(do s)

UNIT-III APPROACH TO DAY TO DAY WORK AND DUTIES.

ShrimadBhagwadGeeta:Chapter2-Verses41,47,48,
Chapter3-Verses13,21,27,35,Chapter6-Verses5,13,17,23,35,
Chapter18-Verses45,46,48.

UNIT-IV STATEMENTS OF BASIC KNOWLEDGE.

ShrimadBhagwadGeeta:Chapter2-Verses 56,62,68
Chapter12 -Verses13,14,15,16,17,18
Personality of Rolemodel. Shrimad Bhagwad Geeta:

UNIT-V CHAPTERS OVERVIEW

Chapter2-Verses 17,Chapter3-Verses36,37,42,
Chapter4-Verses18,38,39
Chapter18 Verses37,38,63

REFERENCE BOOKS:

1. Srimad Bhagavad Gita by Swami Swarupananda Advaita Ashram(Publication Department), Kolkata

2. Bhartrihari s Three Satakam (Niti-sringar-vairagya) by P.Gopinath, RashtriyaSanskrit Sansthanam, New Delhi.

COURSE OUTCOMES:

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students

SANTHIRAM ENGINEERING COLLEGE, NANDYAL (AUTONOMOUS)

R-23 REGULATIONS M.TECH

Highlights of the College

- Received Autonomous Status.
- Accredited by NBA for the Departments of ECE and CSE.
- Accredited by NAAC with Grade-A (3.2 score)
- Recognized as Q-Mentor College by APSCHE, for guiding HEIs for accreditation.
- Listed as one of the Best Engineering College with AA+ Grade by Career 360 in the year 2023.
- Recognized in GOLD CATEGORY by AICTE-CII Survey for the years 2017 & 2018 and also in PLATINUM CATEGORY in the year 2020.
- Received TWO University Gold Medals from JNTUA, Ananthapuramu.
- Received NINE Prathibha Awards from the Govt of A.P.
- SIX Patents were granted and SIX patents were approved under AICTE-KAPILA Scheme.
- Received around 50 Lakhs worth of funding projects under various schemes of UGC, AICTE, IEEE, IE and etc.

SREC VISION:

To become a nucleus for pursuing technical education and pool industrial research and developmental activities with social-conscious and global standards.

SREC MISSION:

- To provide Advanced Educational Programs and prepare students to achieve success and take leading roles in their chosen fields of specialization by arising a self-sustained University.
- To establish postgraduate programs in the current and Advanced Technologies.
- To establish an R&D Consultancy through developing Industry Institute Interaction, building up exceptional infrastructure.
- To propel every individual, realize and act for the technical development of the society.

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