# M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

## COMMON COURSE STRUCTURE & SYLLABI

### SEMESTER – I

<table>
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<tr>
<th>S. No.</th>
<th>Course codes</th>
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**Total** 18
## M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

### COMMON COURSE STRUCTURE & SYLLABI

#### SEMESTER – II

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SEMESTER - III

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SEMESTER - IV

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Course Code: 21D57101

CMOS ANALOG IC DESIGN

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Semester: 1

Course Objectives:
- This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
- Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- Intuitive understanding and real-life applications are emphasized throughout the course.
- To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

Course Outcomes (CO): Student will be able to
- Design MOSFET based analog integrated circuits.
- Analyze analog circuits at least to the first order.
- Appreciate the trade-offs involved in analog integrated circuit design.
- Understand and appreciate the importance of noise and distortion in analog circuits.
- Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
- Solve engineering problems for feasible and optimal solutions in the core area

UNIT - I

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

UNIT - II


UNIT - III

Frequency Response of Amplifiers: General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascade Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT - IV


UNIT - V

Comparators: Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Textbooks:
M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

<table>
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<th>Reference Books:</th>
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Course Code: 21D57102

**CMOS DIGITAL IC DESIGN**

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**Course Objectives:**
- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

**Course Outcomes (CO):** Student will be able to
- Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,
- Estimate Delay and Power of Adders circuits.
- Classify different semiconductor memories.
- Analyze, design and implement combinational and sequential MOS logic circuits.
- Analyze complex engineering problems critically in the domain of digital IC design for conducting research.
- Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.

**UNIT - I**

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

**UNIT - II**

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

**UNIT - III**

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

**UNIT - IV**


**UNIT - V**

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

**Textbooks:**

**Reference Books:**
M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

### Course Objectives:
- Comprehend impact of semiconductor industry on the design of development of integrated circuits.
- Acquaint with clean room technology
- Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
- Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and 45nm technologies
- Understand packaging principles

### Course Outcomes (CO): Student will be able to
- Understand various stages of fabrication
- Understand Various packaging techniques and Design rules.
- Classify various thin films and its characteristics.

#### UNIT - I
**Lecture Hrs:**
**Introduction to Processing:** Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction.

#### UNIT - II
**Lecture Hrs:**
**Photolithography:** Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

#### UNIT - III
**Lecture Hrs:**
**Diffusion & Ion Implantation:** Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

#### UNIT - IV
**Lecture Hrs:**
**Film Depositions and Growth:** Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

#### UNIT - V
**Lecture Hrs:**
**Yield:** Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors.
**Packaging:** Chip characteristics, package functions, package operations.

### Textbooks:

### Reference Books
Course Code: 21D57103b
Program Elective – I

NANOMATERIALS AND NANOTECHNOLOGY

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Course Objectives:
- To understand the basic idea behind the design and fabrication of nano scale systems.
- To understand and formulate new engineering solutions for current problems and technologies for future applications.
- To acquire knowledge on the operation of fabrication and characterization devices to achieve precisely designed systems.

Course Outcomes (CO): Student will be able to
- Understand the basic science behind the design and fabrication of nano scale systems.
- Understand and formulate new engineering solutions for current problems and competing technologies for future applications.
- Make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
- Gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.

UNIT - I

UNIT - II
Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials.Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low Dimensional Carbon-Related Nanomaterials.

UNIT - III

UNIT - IV

UNIT - V
Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane based application, polymer based application.

Textbooks:
COMMON COURSE STRUCTURE & SYLLABI


Reference Books:

# M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

## COMMON COURSE STRUCTURE & SYLLABI

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**Course Objectives:**
- To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- To practice the application of fundamentals of VLSI technologies.
- To optimize the implemented design for area, timing and power by applying suitable constraints.

**Course Outcomes (CO):** Student will be able to
- Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- Practice the application of fundamentals of VLSI technologies.
- Optimize the implemented design for area, timing and power by applying suitable constraints.

## UNIT - I

### Lecture Hrs:


## UNIT - II

### Lecture Hrs:

**Partitioning:** Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.

## UNIT - III

### Lecture Hrs:

**Floor Planning:** Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

## UNIT - IV

### Lecture Hrs:

**Placement and Routing:** Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

**Global Routing and Detailed Routing:** Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

## UNIT - V

### Lecture Hrs:

**Physical Design Automation of FPGAs and MCMs:** FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

**Textbooks:**

**Reference Books:**
M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition
Course Code: 21D57104a
Program Elective – II

Course Objectives:
- To understand the physics of 2-terminal MOS operation and its characteristics
- To understand the physics of 4-terminal MOSFET operation and its characteristics.
- To analyze the SOI MOSFET electrical characteristics.

Course Outcomes (CO): Student will be able to
- Understand the physics of 2-terminal MOS operation and its characteristics
- Understand the physics of 4-terminal MOSFET operation and its characteristics.
- Analyze the SOI MOSFET electrical characteristics.

UNIT - I
Lecture Hrs: 2
2-terminal MOS device: threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT - II
Lecture Hrs: 4
C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit); MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit).

UNIT - III
Lecture Hrs: 4
4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1, 2, 3 and 4).

UNIT - IV
Lecture Hrs: 4
Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer’s model).

UNIT - V
Lecture Hrs: 4
SOI MOSFET: Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

Textbooks:

Reference Books
3. J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009
Course Code | FPGA ARCHITECTURES AND APPLICATIONS
21D57104b | Program Elective – II

Semester 1

Course Objectives:
- To acquire knowledge about various architectures and device technologies of PLD’s.
- To comprehend FPGA Architectures.
- To analyze System level Design and their application for Combinational and Sequential Circuits.
- To familiarize with Anti-Fuse Programmed FPGAs.
- To apply knowledge of this subject for various design applications.

Course Outcomes (CO):
- Acquire knowledge about various architectures and device technologies of PLD’s.
- Comprehend FPGA Architectures.
- Analyze System level Design and their application for Combinational and Sequential Circuits.
- Familiarize with Anti-Fuse Programmed FPGAs.
- Apply knowledge of this subject for various design applications.

UNIT - I


UNIT - II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT - III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT - IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT - V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

Textbooks:

Reference Books:
1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.
Course Code: 21D57104c  
ASIC DESIGN  
Program Elective – II  
Semester I  
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Course Objectives:
- To understand different types of ASICs and their libraries.
- To understand about programmable ASICs, I/O modules and their interconnects.
- To familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

Course Outcomes (CO): Student will be able to
- Understand different types of ASICs and their libraries.
- Understand about programmable ASICs, I/O modules and their interconnects.
- Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT - I  

UNIT - II  
Programmable ASICs and Programmable ASIC Logic Cells: The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT - III  
I/O Cells and Interconnects & Programmable ASIC Design Software: DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT - IV  

UNIT - V  

Textbooks:

Reference Books:
# Course Code: 21D57105

## Course: CMOS ANALOG IC DESIGN LAB

### LTPC

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**Semester:** 1

### Course Objectives:

- To explain the VLSI Design Methodologies using VLSI design tool.
- To grasp the significance of various CMOS analog circuits in full-custom IC Design flow.
- To explain the Physical Verification in Layout Design.
- To fully appreciate the design and analyze of analog and mixed signal simulation.
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

### Course Outcomes (CO):

- Explain the VLSI Design Methodologies using VLSI design tool.
- Grasp the significance of various CMOS analog circuits in full-custom IC Design flow.
- Explain the Physical Verification in Layout Design.
- Fully appreciate the design and analyze of analog and mixed signal simulation.
- Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

### List of Experiments:

- The students are required to design and implement any **TEN** Experiments using CMOS 130nm Technology.
- The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

### Lab Requirements:

**Software:**
- Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator

**Hardware:**
- Personal Computer with necessary peripherals, configuration and operating System.
Course Code: 21D57106

CMOS DIGITAL IC DESIGN LAB

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**Course Objectives:**
- To explain the VLSI Design Methodologies using any VLSI design tool.
- To grasp the significance of various design logic Circuits in full-custom IC Design.
- To explain the Physical Verification in Layout Extraction.
- To fully appreciate the design and analyze of CMOS Digital Circuits.
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

**Course Outcomes (CO):**
- Explain the VLSI Design Methodologies using any VLSI design tool.
- Grasp the significance of various design logic Circuits in full-custom IC Design.
- Explain the Physical Verification in Layout Extraction.
- Fully appreciate the design and analyze of CMOS Digital Circuits.

Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

**List of Experiments:**
The students are required to design and implement the Circuit and Layout of any TEN Experiments using CMOS 130nm Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

**Lab Requirements:**

**Software:**
Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

**Hardware:**
Personal Computer with necessary peripherals, configuration and operating System.
## RESEARCH METHODOLOGY AND IPR

<table>
<thead>
<tr>
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### Course Objectives:
- Identify an appropriate research problem in their interesting domain.
- Understand ethical issues understand the Preparation of a research project thesis report.
- Understand the Preparation of a research project thesis report
- Understand the law of patent and copyrights.
- Understand the Adequate knowledge on IPR

### Course Outcomes (CO): Student will be able to
- Analyze research related information
- Follow research ethics
- Understand that today’s world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

### UNIT - I

Lecture Hrs:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

### UNIT - II

Lecture Hrs:

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

### UNIT - III

Lecture Hrs:


### UNIT - IV

Lecture Hrs:


### UNIT - V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

### Textbooks:
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”

### Reference Books:
Course Code: CMOS MIXED SIGNAL IC DESIGN

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Semester II

Course Objectives:
- To demonstrate first order filter with least interference
- To extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- To design different A/D, D/A, modulators, demodulators and different filter for real time applications

Course Outcomes (CO): Student will be able to
- Demonstrate first order filter with least interference
- Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- Design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT - I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

UNIT – II

Phased Lock Loop (PLL) : Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT - III

Data Converter: Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT - IV


UNIT - V

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A

Textbooks:

Reference Books:
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inter science, 2005.
Course Code  PHYSICAL DESIGN AUTOMATION  L  T  P  C
21D57202  3  0  0  3

Course Objectives:
- To understand relation between automation algorithms and constraints posed by VLSI technology.
- To adopt algorithms to meet critical design parameters.
- To design area efficient logics by employing different routing algorithms and shape functions.
- To simulate and synthesis different combinational and sequential logics.

Course Outcomes (CO): Student will be able to
- Understand relation between automation algorithms and constraints posed by VLSI technology.
- Adopt algorithms to meet critical design parameters.
- Design area efficient logics by employing different routing algorithms and shape functions.
- Simulate and synthesis different combinational and sequential logics.

UNIT - I
VLSI Design Automation Tools: Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT - II

UNIT - III
Floor planning and routing: Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT - IV
Simulation and Logic Synthesis: Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis.

UNIT - V
High-Level Synthesis: Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

Textbooks:

Reference Books:
Course Code: 21D57203a
Program Elective – III

Course Objectives:
- To understand the concepts of faults and testing in SoC
- To implement the faults using simulation tools
- To analyze BIST systems

Course Outcomes (CO): Student will be able to
- Understand the concepts of faults and testing in SoC
- Implement the faults using simulation tools
- Analyze BIST systems

UNIT - I

UNIT - II

UNIT - III

UNIT - IV
Lecture Hrs: Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V
Lecture Hrs: Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Textbooks:

Reference Books:
Course Code: 21D57203b
Program Elective – III
Semester II

<table>
<thead>
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<th>Course Objectives:</th>
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<tbody>
<tr>
<td>• To understand different types of memories, their architectural and different packing techniques of memories.</td>
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<td>• To build fault models for memory testing.</td>
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<td>• To analyze different parameters that lead malfunctioning of memories.</td>
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<td>• To design reliable memories with efficient architecture to improve processes times and power.</td>
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Course Outcomes (CO): Student will be able to

<table>
<thead>
<tr>
<th>Unit</th>
<th>Lecture Hrs:</th>
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<tbody>
<tr>
<td><strong>UNIT - I</strong></td>
<td>Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.</td>
</tr>
<tr>
<td><strong>UNIT - II</strong></td>
<td>Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture</td>
</tr>
<tr>
<td><strong>UNIT - III</strong></td>
<td>Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory.</td>
</tr>
<tr>
<td><strong>UNIT - V</strong></td>
<td>Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory</td>
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### COMMON COURSE STRUCTURE & SYLLABI

Packaging Future Directions.

<table>
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<th>Textbooks:</th>
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<th>Reference Books:</th>
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**Course Code**: 21D57203c  
**Program Elective – III**  
**Semester**: II

### Course Objectives:
- To understand the basic concepts of MEMS technology and working of MEMS devices.
- To understand and select different materials for current MEMS devices and competing technologies for future applications.
- To understand the concepts of fabrication process of MEMS, Design and Packaging Methodology.
- To analyze the various fabrication techniques in the manufacturing of MEMS Devices.

### Course Outcomes (CO):
- Understand the basic concepts of MEMS technology and working of MEMS devices.
- Understand and select different materials for current MEMS devices and competing technologies for future applications.
- Understand the concepts of fabrication process of MEMS, Design and Packaging Methodology.
- Analyze the various fabrication techniques in the manufacturing of MEMS Devices.

### Textbooks:
1. An Introduction to Micro electromechanical Systems Engineering; 2nd Edition by N.Maluf, K Williams; Publisher: Artech House Inc
2. Practical MEMS - by Ville Kaajakari; Publisher: Small Gear Publishing
3. Micro system Design - by S. Senturia; Publisher: Springer

### Reference Books:
# COMMON COURSE STRUCTURE & SYLLABI

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<td>2.</td>
<td>Fundamentals of Micro fabrication - by M. Madou; Publisher: CRC Press; 2nd edition</td>
</tr>
<tr>
<td>3.</td>
<td>Micro Electro Mechanical System Design - by J. Allen; Publisher: CRC Press</td>
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<tr>
<td>4.</td>
<td>Micro machined Transducers Sourcebook - by G. Kovacs; Publisher: McGraw-Hill</td>
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# M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

## COMMON COURSE STRUCTURE & SYLLABI

<table>
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<th>Course Code</th>
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| Semester | II |

### Course Objectives:
- To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- To implement Low power design approaches for system level and circuit level measures.
- To design low power adders, multipliers and memories for efficient design of systems.

### Course Outcomes (CO):
- Student will be able to
  - Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
  - Implement Low power design approaches for system level and circuit level measures.
  - Design low power adders, multipliers and memories for efficient design of systems.

### UNIT - I

**Lecture Hrs:**

**Fundamentals:**

### UNIT - II

**Lecture Hrs:**

**Low-Power Design Approaches:**

### UNIT - III

**Lecture Hrs:**

**Low-Voltage Low-Power Adders:**

### UNIT - IV

**Lecture Hrs:**

**Low-Voltage Low-Power Multipliers:**
- Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

### UNIT - V

**Lecture Hrs:**

**Low-Voltage Low-Power Memories:**

### Textbooks:
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

### Reference Books:
Course Code: 21D57204b  
Program Elective – IV  
Semester II

Course Objectives:
- To apply the Knowledge in IOT Technologies and Data management.
- To determine the values chains Perspective of M2M to IOT.
- To implement the state of the Architecture of an IOT.
- To compare IOT Applications in Industrial & real world.
- To demonstrate knowledge and understand the security and ethical issues of an IOT.

Course Outcomes (CO):
- Apply the Knowledge in IOT Technologies and Data management.
- Determine the values chains Perspective of M2M to IOT.
- Implement the state of the Architecture of an IOT.
- Compare IOT Applications in Industrial & real world.
- Demonstrate knowledge and understand the security and ethical issues of an IOT.

UNIT - I  
Lecture Hrs:

IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT - II  
Lecture Hrs:
IoT Protocols: IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT - III  
Lecture Hrs:
Design and Development: Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT - IV  
Lecture Hrs:
Data Analytics and Supporting Services: Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT - V  
Lecture Hrs:

Textbooks:
M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

2. Internet of Things – A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press, 2015

Reference Books:

1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.
# Course Objectives:
- To study the existing architectures suitable for VLSI.
- To understand the concepts of folding and unfolding algorithms and applications.
- To design new architectures suitable for VLSI.
- To implement fast convolution algorithms.

# Course Outcomes (CO): Student will be able to
- Study the existing architectures suitable for VLSI.
- Understand the concepts of folding and unfolding algorithms and applications.
- Design new architectures suitable for VLSI.
- Implement fast convolution algorithms.

## UNIT - I
**Introduction to DSP:** Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

## UNIT - II
**Folding and Unfolding:** Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

## UNIT - III
**Systolic Architecture Design:** Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

## UNIT - IV
**Fast Convolution:** Introduction – Cook - Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

## UNIT - V
**Low Power Design:** Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

### Textbooks:

### Reference Books:
**Course Code**

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<tr>
<th>Course Code</th>
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**Semester** II

**Course Objectives:**
- To design and simulate op-amp for given specifications
- To design and simulate data converter for given specifications
- To design and simulate PLL and VCO for given specifications
- To understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

**Course Outcomes (CO):**
- Design and simulate op-amp for given specifications
- Design and simulate data converter for given specifications
- Design and simulate PLL and VCO for given specifications
- Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

**List of Experiments:**
The students are required to design and implement the Circuit and Layout of the following Experiments using CMOS 130nm Technology.

**Cycle 1:**
1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   a. Two stage cross coupled clamped comparator
   b. Strobed Flip-flop
3) Data converter

**Cycle 2:**
1) Switched capacitor circuits
   a. Parasitic sensitive integrator
   b. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Band gap reference circuit
5) Layouts of All the circuits Designed and Simulated

**Software:**
Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

**Hardware:**
Personal Computer with necessary peripherals, configuration and operating System.

**References:**
### Course Objectives:
- To learn the implementation of different Physical Design Automation algorithms
- To implement different graph algorithms
- To implement different partitioning algorithms
- To implement different floor planning algorithms
- To implement different routing algorithms

### Course Outcomes (CO):
- Learn the implementation of different Physical Design Automation algorithms
- Implement different graph algorithms
- Implement different partitioning algorithms
- Implement different floor planning algorithms
- Implement different routing algorithms

### List of Experiments:
#### Cycle 1:
1) Graph algorithms
   a) Graph search algorithms
      i. Depth first search
      ii. Breadth first search
   b) Spanning tree algorithm
      i. Kruskal’s algorithm
   c) Shortest path algorithm
      i. Dijkstra algorithm
      ii. Floyd–Warshall algorithm
   d) Steiner tree algorithm
2) Computational geometry algorithm
   a) Line sweep method
   b) Extended line sweep method

#### Cycle 2:
3) Partitioning algorithms
   a) Group migration algorithms
      I. Kernighan–Lin algorithm
      II. Extensions of Kernighan-Lin algorithm
         i) Fiduccias–Mattheyses algorithm
         ii) Goldberg and Burstein algorithm
   b) Simulated annealing and evolution algorithms
      i. Simulated annealing algorithm
      ii. Simulated evolution algorithm

#### Cycle 3:
4) Floor planning algorithms
   i) Constraint based methods
   ii) Integer programming based methods
   iii) Rectangular dualization based methods
   iv) Hierarchical tree based methods
M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

v) Simulated evolution algorithms
vi) Time driven Floor planning algorithms

5) Routing algorithms
   I) Two terminal algorithms
      a) Maze routing algorithms
         i) Lee’s algorithm
         ii) Soukup’s algorithm
         iii) Hadlock algorithm
      b) Line-Probe algorithm
      c) Shortest path based algorithm
   II) Multi terminal algorithm
      a) Steiner tree based algorithm
         i) SMST algorithm
         ii) Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

Text Books:
Course Code: 21D57301a  
Program Elective – V  
Semester: III

Course Objectives:
- To demonstrate in-depth knowledge in BiCMOS Technology.
- To analyze complex engineering problems critically for conducting research in BiCMOS Technology.
- To solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
- To realize different digital circuits using BiCMOS Technology

Course Outcomes (CO): Student will be able to
- Demonstrate in-depth knowledge in BiCMOS Technology.
- Analyze complex engineering problems critically for conducting research in BiCMOS Technology.
- Solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
- Realize different digital circuits using BiCMOS Technology

UNIT - I  

UNIT - II  
Device Design Considerations: Design Considerations for MOSFET's, Design Considerations for Bipolar Transistors, BiCMOS Device Design Considerations.

BiCMOS Device Scaling: MOS Device Scaling, Bipolar Device Scaling.

UNIT - III  

UNIT - IV  
BiCMOS Digital Integrated Circuits: BiMOS Totem-Pole Inverter: DC Characteristics, Transient Analysis, Delay Dependence on the Device Parameters, BiCMOS Circuit Design, Comparing CMOS and BiCMOS Inverters Speed, BiCMOS Gates.

UNIT - V  
BiCMOS Digital Circuit Applications: Adders, Multiplier, Random Access Memory, Programmable Logic Arrays, BiCMOS Logic Cells, BiCMOS Gate Arrays.

Textbooks:

Reference Books:
3. Klaas Jan de Langen, Johan Huijsing, Compact Low-Voltage and High-Speed CMOS, BiCMOS and Bipolar Operational Amplifiers, Springer Science
# M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

## COMMON COURSE STRUCTURE & SYLLABI

<table>
<thead>
<tr>
<th>Course Code</th>
<th>OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN (Program Elective – V)</th>
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**Semester** III

### Course Objectives:
- To understand basics of statistical modeling
- To analyze performance of CMOS circuits with respect to power, area and speed
- To acquire complete knowledge regarding the various algorithms used for optimization of power and area

### Course Outcomes (CO): Student will be able to
- Understand basics of statistical modeling
- Analyze performance of CMOS circuits with respect to power, area and speed
- Acquire complete knowledge regarding the various algorithms used for optimization of power and area

#### UNIT - I
**Lecture Hrs:**
- **Statistical Modeling:** Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom’s model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

#### UNIT - II
**Lecture Hrs:**
- **Statistical Performance, Power and Yield Analysis:** Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

#### UNIT - III
**Lecture Hrs:**
- **Convex Optimization:** Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floorplanning, wiresizing, Approximation and fitting-Monomial fitting, Maxmonomial fitting, Polynomial fitting.

#### UNIT - IV
**Lecture Hrs:**

#### UNIT - V
**Lecture Hrs:**

### Textbooks:

### Reference Books:
# M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

## COMMON COURSE STRUCTURE & SYLLABI

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<th>Course Code</th>
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<td>Program Elective – V</td>
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### Course Objectives:
- To understand the basics related to SoC architecture and different approaches related to SoC Design.
- To select an appropriate robust processor for SoC Design.
- To select an appropriate memory for SoC Design.
- To realize real time case studies.

### Course Outcomes (CO):
- Understand the basics related to SoC architecture and different approaches related to SoC Design.
- Select an appropriate robust processor for SoC Design.
- Select an appropriate memory for SoC Design.
- Realize real time case studies.

### UNIT - I


### UNIT - II

**Processors:** Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors.

### UNIT - III

**Memory Design for SOC:** Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

### UNIT - IV

**Interconnect, Customization and Configurability:** Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

**SOC Customization:** An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

### UNIT - V

**Application Studies / Case Studies:** SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

### Textbooks:

### Reference Books:
### M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

**COMMON COURSE STRUCTURE & SYLLABI**

| 2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM. |
AUDIT COURSE-I
Course Code: 21DAC101a

**ENGLISH FOR RESEARCH PAPER WRITING**

<table>
<thead>
<tr>
<th>Course Code</th>
<th>English for Research Paper Writing</th>
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**Semester I**

**Course Objectives:** This course will enable students:

- Understand the essentials of writing skills and their level of readability
- Learn about what to write in each section
- Ensure qualitative presentation with linguistic accuracy

**Course Outcomes (CO):** Student will be able to

- Understand the significance of writing skills and the level of readability
- Analyze and write title, abstract, different sections in research paper
- Develop the skills needed while writing a research paper

**UNIT - I**

Overview of a Research Paper - Planning and Preparation - Word Order - Useful Phrases - Breaking up Long Sentences - Structuring Paragraphs and Sentences - Being Concise and Removing Redundancy - Avoiding Ambiguity

**UNIT - II**


**UNIT - III**


**UNIT - IV**

Key skills needed for writing a Title, Abstract, and Introduction

**UNIT - V**

Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions

**Suggested Reading**

2. Model Curriculum of Engineering & Technology PG Courses [Volume-I]
Course Objectives: This course will enable students:

- Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluatedisaster risk reduction and humanitarian response policy and practice from Multiple perspectives.
- Develop an understanding of standard of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

UNIT - I

Introduction:
Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

UNIT - II

Repercussions of Disasters and Hazards:

UNIT - III

Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT - IV

Risk Assessment Disaster Risk:

UNIT - V

Disaster Mitigation:
Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation, Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Suggested Reading
M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Company., Sahni, Pardeep Et. Al. (Eds.), "Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
Course Code: 21DAC101c  
Sanskrit for Technical Knowledge  

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**Course Objectives:** This course will enable students:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop logic in mathematics, science & other subjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge
- Knowledge from ancient literature

**Course Outcomes (CO):** Student will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood
- Being a logical language will help to develop logic in students

**UNIT - I**

Alphabets in Sanskrit,

**UNIT - II**

Past/Present/Future Tense, Simple Sentences

**UNIT - III**

Order, Introduction of roots

**UNIT - IV**

Technical information about Sanskrit Literature

**UNIT - V**

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

**Suggested Reading**

1. “Abhyasputakam” – Dr. Vishwas, Sanskrit-Bharti Publication, New Delhi
2. “Teach Yourself Sanskrit” Prathama Deeksha- VempatiKutumbshastri, RashtriyaSanskrit Sansthanam, New Delhi Publication
3. “India’s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd., New Delhi
M.TECH. IN VLSI/VLSI DESIGN/VLSI SYTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

AUDIT COURSE-II
**Course Objectives:** This course will enable students:

- Review existing evidence on the development of pedagogical practices and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

**Course Outcomes (CO):** Student will be able to

**Students will be able to understand:**

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practice) and the school curriculum and guidance materials best support effective pedagogy?

**UNIT - I**

**Introduction and Methodology:** Aims and rationale, Policy background, Conceptual frame work and terminology. Theories of learning, Curriculum, Teacher education, Conceptual framework, Research questions. Overview of methodology and Searching.

**UNIT - II**

**Thematic overview:** Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

**UNIT - III**


**UNIT - IV**

**Professional development:** alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

**UNIT - V**

**Research gaps and future directions:** Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

**Suggested Reading**


COMMON COURSE STRUCTURE & SYLLABI

<table>
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<tr>
<th>Course Code</th>
<th>STRESSMANAGEMENT BY YOGA</th>
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Course Objectives: This course will enable students:
- To achieve overall health of body and mind
- To overcome stress

Course Outcomes (CO): Student will be able to
- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT - I
Definitions of Eight parts of yog.(Ashtanga)

UNIT - II
Yam and Niyam.

UNIT - III
Do’sand Don’t’s in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigrahaii
   Shaucha, santosh, tapa, swadhay, ishwarpranidhan

UNIT - IV
Asan and Pranayam

UNIT - V
i) Various yogasand their benefitsformind & body
ii) Regularization of breathing techniques and its effects - Types ofpranayam

Suggested Reading
1.“Yogic Asanas for Group Training-Part-I”: Janardan Swami Yogabhayasi Mandal, Nagpur
2.“Rajyoga or conquering the Internal Nature” by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata
Course Code: 21DAC201c  
**PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS**

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Semester II

**Course Objectives:** This course will enable students:
- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

**Course Outcomes (CO):** Student will be able to
- Study of Shrimad-Bhagavad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

**UNIT - I**

Neetisatakam - Holistic development of personality
Verses: 19, 20, 21, 22 (wisdom)
Verses: 29, 31, 32 (pride & heroism)
Verses: 26, 28, 63, 65 (virtue)

**UNIT - II**

Neetisatakam - Holistic development of personality
Verses: 52, 53, 59 (don’ts)
Verses: 71, 73, 75, 78 (do’s)

**UNIT - III**

Approach to day to day work and duties.
Shrimad Bhagwad Geeta: Chapter 2 - Verses 41, 47, 48,
Chapter 3 - Verses 13, 21, 27, 35,
Chapter 4 - Verses 5, 13, 17, 23, 35,
Chapter 18 - Verses 45, 46, 48.

**UNIT - IV**

Statements of basic knowledge.
Shrimad Bhagwad Geeta: Chapter 2 - Verses 56, 62, 68
Chapter 12 - Verses 13, 14, 15, 16, 17, 18
Personality of Rolemodel: Shrimad Bhagwad Geeta:

**UNIT - V**

Chapter 2 - Verses 17, Chapter 3 - Verses 36, 37, 42,
Chapter 4 - Verses 18, 38, 39
Chapter 18 - Verses 37, 38, 63

**Suggested Reading**

1. “Srimad Bhagavad Gita” by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari’s Three Satakam (Niti-sringar-vairagya) by P. Gopinath, Rashtriya Sanskrit Sansthana, New Delhi.
OPEN ELECTIVE
M.TECH. IN VLSI/VLSI DESIGN/VLSI SYSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

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Course Objectives:
- To know about Industrial safety programs and toxicology, Industrial laws, regulations and source models
- To understand about fire and explosion, preventive methods, relief and its sizing methods
- To analyse industrial hazards and its risk assessment.

Course Outcomes (CO): Student will be able to
- To list out important legislations related to health, safety and environment.
- To list out requirements mentioned in factories act for the prevention of accidents.
- To understand the health and welfare provisions given in factories act.

UNIT - I
Lecture Hrs: Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc. Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT - II
Lecture Hrs: Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT - III

UNIT - IV
Lecture Hrs: Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment’s like, i. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT - V

Textbooks:

Reference Books:
<table>
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<tr>
<th>Course Code</th>
<th>BUSINESS ANALYTICS</th>
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Semester III

### Course Objectives:
- The main objective of this course is to give the student a comprehensive understanding of business analytics methods.

### Course Outcomes (CO):
- Students will demonstrate knowledge of data analytics.
- Students will demonstrate the ability to think critically in making decisions based on data and deep analytics.
- Students will demonstrate the ability to use technical skills in predictive and prescriptive modeling to support business decision-making.
- Students will demonstrate the ability to translate data into clear, actionable insights.

### UNIT - I
- **Lecture Hrs:**
- Business Analysis: Overview of Business Analysis, Overview of Requirements, Role of the Business Analyst
- Stakeholders: the project team, management, and the front line, Handling Stakeholder Conflicts

### UNIT - II
- **Lecture Hrs:**

### UNIT - III
- **Lecture Hrs:**

### UNIT - IV
- **Lecture Hrs:**
- Finalizing Requirements: Presenting Requirements, Socializing Requirements and Gaining Acceptance, Prioritizing Requirements, Managing Requirements Assets: Change Control, Requirements Tools

### UNIT - V
- **Lecture Hrs:**
- Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data Journalism

### Textbooks:
1. Business Analysis by James Cadle et al.
2. Project Management: The Managerial Process by Erik Larson and, Clifford Gray

### Reference Books:
2. Business Analytics by James Evans, persons Education.
## Course Outcomes (CO): Student will be able to

- To know about overview of Energy to waste and classification of waste.
- To acquire knowledge on bio mass pyrolysis, gasification, combustion and conversion process in detail.
- To gain knowledge on properties of biogas, biomass resources and programmes to convert waste to energy in India.

### UNIT - I

Lecture Hrs: 10

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digesters.

### UNIT - II

Lecture Hrs: 10


### UNIT - III

Lecture Hrs: 12


### UNIT - IV

Lecture Hrs: 12

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

### UNIT - V

Lecture Hrs: 10

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification- pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

### Textbooks:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 2018

### Reference Books:

## COMMON COURSE STRUCTURE & SYLLABI

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<th>Online Learning Resources:</th>
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<td><a href="https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ch13/">https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ch13/</a></td>
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& Sons, 1996